Amendments to the Claims:

A clean version of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121(c) (3). This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) A circuit arrangement as claimed in claim 15[[1]], characterized in that the amplification factor (n) is approximately 5.

3. (Currently Amended) A circuit arrangement as claimed in claim [[1]]15, characterized in that the signal is amplified in the pnp current mirror (16) or in the npn transistor current mirror (14).

4. (Currently Amended) A circuit arrangement as claimed in claim [[1]]15 characterized in that the high voltage source (30) supplies a voltage of the order of approximately 12 V.

5. (Currently Amended) A circuit arrangement as claimed in claim [[1]]15, characterized in that the input (12) of the adapter circuit (10) is preceded by at least one supply or driver circuit (40) by which the low current (I_i) input signal can be applied to the adapter circuit (10).

6. (Original) A circuit arrangement as claimed in claim 5, characterized in that the supply or driver circuit (40) is connected to at least one low voltage source (42).

7. (Original) A circuit arrangement as claimed in claim 6, characterized in that the low voltage source (42) supplies a voltage of the order of approximately 1 V to approximately 3.3 V.

8. (Currently Amended) A circuit arrangement as claimed in claim [[1]] 15, characterized in that

- the npn transistor arrangement (14) is constituted as an npn current mirror and/or particularly as an NMOS current mirror (NMOS = N-channel Metal Oxide Semiconductor = N-type Metal Oxide Semiconductor); and/or

- the pnp transistor arrangement (16) is constituted as a pnp current mirror and/or particularly as a PMOS current mirror (PMOS = P-channel Metal Oxide Semiconductor = P-type Metal Oxide Semiconductor).

9. (Currently Amended) A circuit arrangement as claimed in [[1]]15, characterized in that the output (18) of the adapter circuit (10) precedes at least a resistor (50) for converting the higher current (I_o) output signal into a higher voltage (U_o) output signal.

10. (Original) A circuit arrangement as claimed in claim 9, characterized in that the resistor (50) has a value of approximately 1 kΩ.

11. (Currently Amended) A circuit arrangement as claimed in claim [[1]]15, characterized in that the output (18) of the adapter circuit (10) precedes at least a SCART (= Syndicat des Constructeurs d'Appareils Radio Receteurs et Televiseurs) output (70).

12. (Currently Amended) A circuit arrangement as claimed in [[1]]15, characterized in that the adapter circuit (10) is multi-staged and/or more than one adapter circuit (10) is provided.

13. (Original) A circuit arrangement as claimed in claim 12, characterized in that eight npn transistors (14) and 24 pnp transistors (16) are provided, and in that the four-stage adapter circuit (10) or the four adapter stages (10) precede a resistor (50).

14. (Currently Amended) A television, multimedia, radio or video recording device comprising at least a circuit arrangement (100) as claimed in claim [[1]]15.

15. (New) A circuit arrangement, comprising:
at least one adapter circuit (10), which amplifies an analog input signal of a low current (I_i) by an amplification factor (n) into a particularly analog output signal of a higher current (I_o), the at least one adapter circuit further comprising:

an input (12), which corresponds to a range of low voltages (U_i);
an output (18), which corresponds to a range of higher voltages (U_o);
at least one npn transistor current mirror (14); and
at least one pnp transistor current mirror (16) arranged in series with the npn transistor current mirror (14), and connected to at least one high voltage source (30), wherein the at least one pnp transistor current mirror amplifies the input signal, which is received from the at least one npn transistor current mirror.